AUD-ESP-00458

IA610 SmartMic Always-On Voice Wake Audio Processor

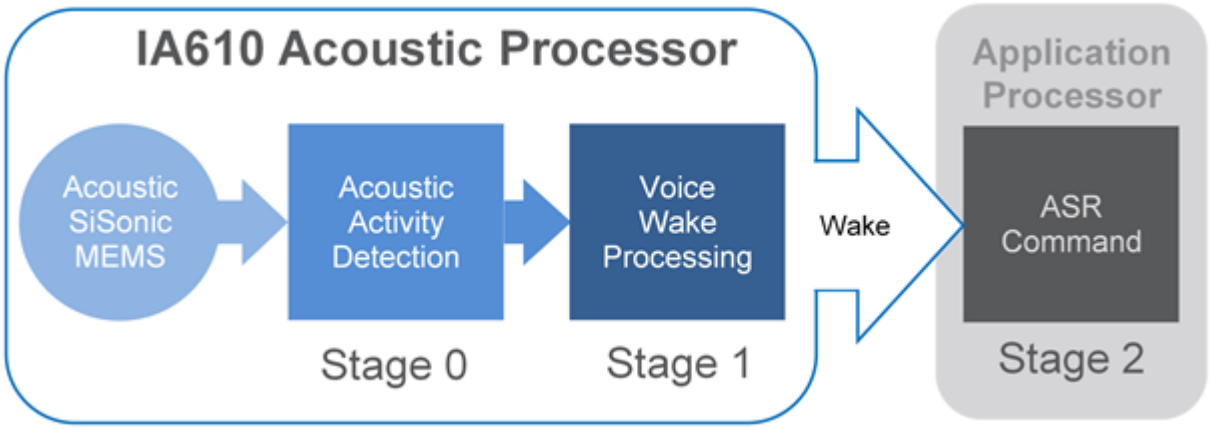
The IA610 SmartMic is an “always-on” audio processor featuring high-performance keyword recognition, a 43 MHz audio-optimized DSP, and Knowles’ high-performance acoustic SiSonicTM MEMS microphone technology in a single, miniature, bottom-port microphone package. The solution pushes the system performance to ultra-low power with its custom core design and optimized instruction set. It accelerates time-to-market with its highly integrated combination of hardware, software, and firmware.

Product Features

- Ultra-low power, high-accuracy voice wake and Voice ID keyword recognition
- On-board buffering and high-speed interfaces offer seamless, continuous voice wake operation
- Ultra-low-power “always on” acoustic activity detector (AAD), capable of waking the embedded DSP
- Integrated power management, offering dynamic voltage scaling for optimal power consumption in a variety of use cases
- Flexible audio and communication interfaces:
  - Standard PDM, I^2S, and TDM
  - SPI/UART/I^2C
- High-performance acoustic SiSonic MEMS with ±1 dB matched sensitivity, 65.5 dB SNR, and 132.5 dB SPL AOP
- Packaged in bottom-port SPH 3.50 x 2.65 x 0.98 mm

Typical Applications

- Smartphones
- Wireless Headsets
- Battery-Powered Smart Speakers
- Laptop Computers
- Tablets
- Remote Controls



Absolute Maximum Ratings

Parameter	Absolute Maximum Ratings	Units
Vdd to Ground	-0.5, +5.0	V
DATA, CLOCK, SELECT to Ground	-0.3, +5.0	V
Input Current	±5	mA
Short Circuit to/from DATA	Indefinite to Ground or Vdd	sec
Storage Temperature	-40 to +100	ºC
Operating Temperature	-40 to +85	ºC

Stresses exceeding these Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only. Functional operation at these or any other conditions beyond those indicated under Acoustic and Electrical Specifications is not implied. Exposure beyond those indicated under Acoustic and Electrical Specifications for extended periods may affect device reliability. for extended periods may affect device reliability.

Table of Contents

Chapter 1: Overview

This overview of the IA610 SmartMic describes the features of the IA610 and typical applications.

The Knowles IA610 SmartMic is a flexible, low-power, and highly integrated voice and audio processor system for battery-powered applications. The IA610 includes:

- Excellent electro-acoustic performance:
  - Recording/Voice-Call performance: 65.5 dB SNR and 132.5 dB AOP.
  - Low-power mode (voice wake and always-on) performance: 64.5 dB SNR and 116.5 dB AOP.
- An advanced, Knowles audio-optimized DSP sub-system:
  - Runs compute-intensive audio processing algorithms with very low-power consumption.
  - Provides an efficient interface between custom software and the digital audio stream data.
- A System Control Unit (SCU) that handles booting, reset, and power management states such as deep-sleep, retention sleep, AAD, keyword detection mode, and many others to optimize power performance.
- A flexible internal clock generation and routing system.
- Integrated audio interfaces for PDM and I^2S/TDM digital audio data.
- A variety of control interfaces, including UART, SPI slave, or I^2C slave. All have audio streaming capability.
- High-performance and ultra-low power voice wakeup capabilities:
  - Supports AAD mode (see Section 4.2, Voice Wake Mode,for details) for optimal low-power performance.
  - Detection of either pre-defined, non-trained keywords (OEM) or pre-defined, user-trained (VID) keywords.
  - Continuous Voice Wake for seamless transition from Voice Wake to a command phrase that follows (see Section 4.3, Continuous Voice Wake, for details).
  - A comprehensive reference trainer for VID keywords.
- AuVid firmware build tool:
  - Knowles provides AuViD, a comprehensive tool for firmware development and testing, as well as IA610 system configuration.
  - AuViD provides configuration, debug, and design capabilities for engineers. System capabilities include audio streaming, as well as system and route configuration. It can be used:
    - Offline to define the options in the firmware;
    - connected to the host directly for run-time debug using a host interface (I2C, UART, or SPI); or
    - connected using an Android Proxy bridge.

The IA610 is optimized for low-power operation in a wide array of applications, including mobile devices.

The IA610 comes with a set of reference drivers for common operating systems and platforms; this makes for easy integration and fast time-to-market. The operating system software is written for the latest Android release and supports communication/data transport over the interfaces listed in Table 1.

Table 1 Android System Interfaces

Control Message	Audio Ports	Audio Upload
I²C	I²S	I²S
UART	I²S	I²S
SPI	PDM	SPI
UART	PDM	UART
I²C	PDM	I²C

Only one control interface can be used at a time. See Section 5.1.3, Control Interfaces, for details.

Chapter 2: Typical Application Block Diagrams

Figure 1 and Figure 2 show typical block diagrams for a host system using the IA611. (For pin configuration per boot mode, see Table 18 and Table 1.)

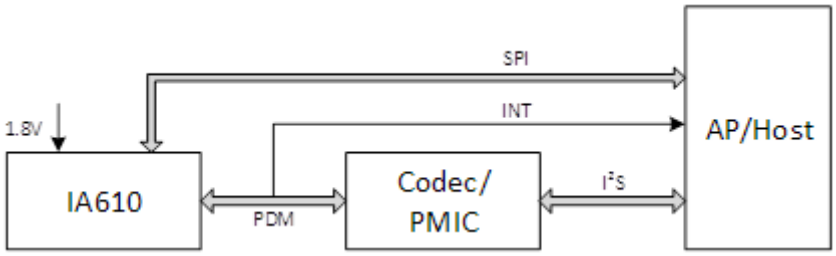


Figure 1 Application Schematic for a Host System using I2S with SPI

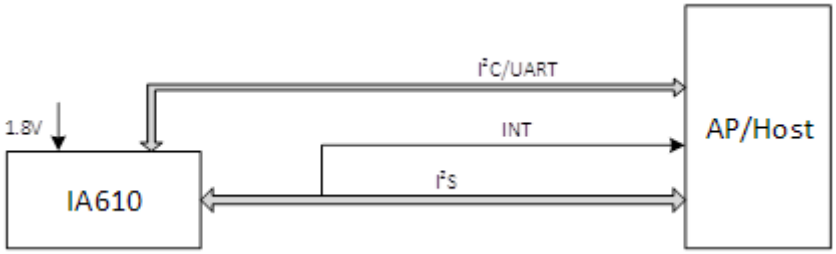


Figure 2 Application Schematic for a Host System using I²S and I²C or UART

Chapter 3: SmartMic Description

3.1 IA610 Subsystem

Figure 3 shows the IA610's major modules, which are:

- Low-noise, dual-MEMS transducer microphone element.
- Advanced high-performance and power-optimized analog signal path.
- Ultra-low-power and high-performance DSP sub-system.
- Digital Audio Interface module that provides configurable serial digital audio ports, each supports streaming a wide variety of data formats, including PDM, I2S, or TDM.
- SPI, UART, and I2C Host Interfaces, including (IA610 version):
  - Communication with the host.
  - A channel for high-speed firmware downloads.
  - Audio data bursting for Voice Wake or diagnostic purposes.
- System Control Unit (SCU) that handles booting, reset, and power-management states such as deep-sleep mode.
- Internal clock control module that generates internal clock signals and masters output clocks; it also locks internal time bases to externally-provided clocks.
- System interrupt module, which provides:
  - Interrupt to host for keyword detection events.
  - Event handling to the IA610 for wakeup from host.

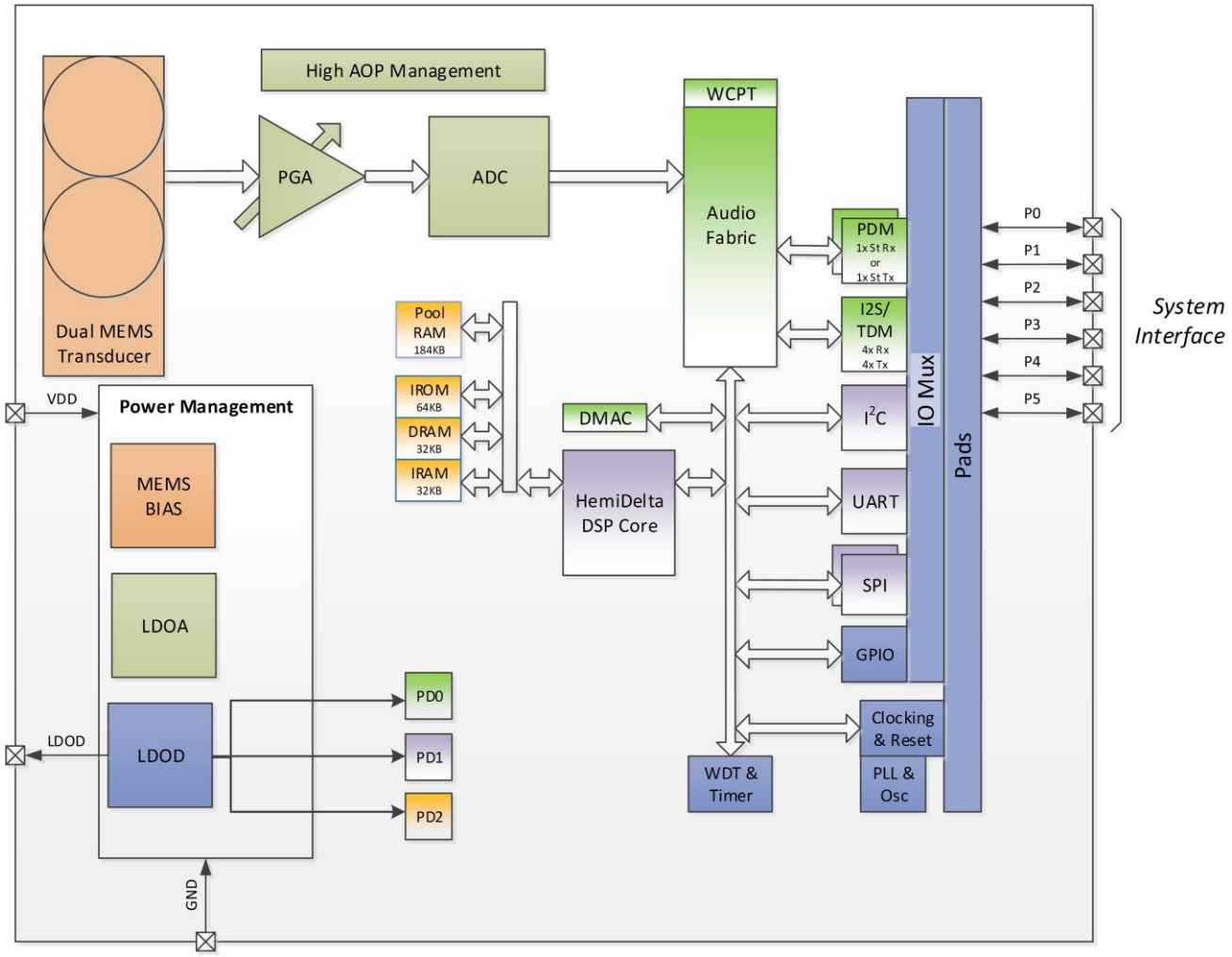


Figure 3 IA610 SmartMic Block Diagram

3.2 DSP Subsystem

The DSP subsystem is comprised of a HemiDelta (HMD) processor, digital decimation and interpolation filters, the Audio Fabric, and memory.

3.2.1 Hemi Delta Processor (HMD)

The HMD is a lower-power digital signal processor that is optimized for frame-based processing. Its features include:

- 64-bit instruction memory access (maximum instruction size: 64 bits).
- 64-bit data memory access (maximum register width: 64 bits).
- Main data type: 32-bit float (AFLOAT).
- Main vector register file: 16 vector registers (two 32-bit lanes each).
- Permutation registers to support load/store, permute, and arithmetic instructions.
- Dual issue instruction bundles.
- Vector and scalar instructions.

- Four MACs (real and complex arithmetic support).
- Nonlinear functions: arc tangent, cosine, sine, log, exponential, inverse, inverse square root, and sigmoid (exponential approximation).
- Added acceleration:
  - FFT
  - Peak finding
  - DNNs (eight 8-bit x 8-bit, fixed-point MACs)

3.2.2 Digital Filters

The IA610 digital filters allow use of Pulse Density Modulation (PDM) audio data. There are four receive decimation filter chains, and two transmit interpolation filter chains. The decimation filters support one-bit PDM input oversampled audio data from digital microphones and codec interfaces. The interpolation filters generate one-bit PDM output oversampled audio data that can go to a speaker or codec.

3.2.3 Audio Fabric

The Audio Fabric is a memory mapped interface that allows any processor to access data efficiently from the various audio interfaces supported by the chip, such as I^2S/TDM, PDM. Each audio interface converts input data into a common 32-bit integer format; it is synchronized into the processor clock domain from the native audio clock before being multiplexed in the Audio Fabric into generic N-channel logical streams of audio data. Similarly, each audio interface can convert 32-bit integer format data into the encoding required for transmission. The audio fabric has support for a low-latency path; it also has connections to the wall clock/presentation timers unit to allow them to capture “timestamps” of audio data.

3.2.4 Memory

The IA610 has a total of 248 KB of RAM, divided as:

- 64 KB dedicated memory: 32 KB instruction and 32 KB data.
- 184 KB shared memory pool.
- Of the total 248 KB memory, 168 KB is reserved for custom algorithm use.

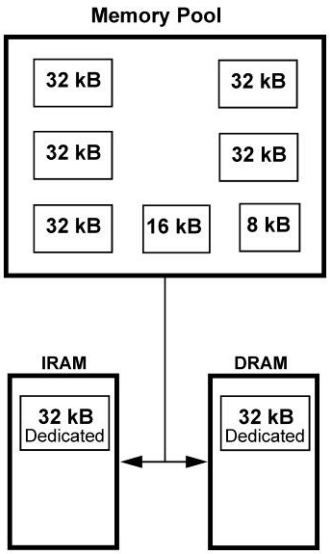


Figure 4 Memory Pool Structure

3.2.5 Audio Interfaces

The IA610 audio processor supports the following transfer of audio data:

- Master/Slave I²S/TDM.
- Two PDM output channels.

3.2.5.1 Digital Microphone PDM Output Interface

The IA610 has a single PDM output signal that can be used to transmit two audio channels. The data for one of the two audio channels is transmitted on each clock edge, as shown in Figure 5. In PDM output mode, the clock can be configured as input (slave) or output (master). If it is programmed as input, Table 7 lists the supported frequency ranges. If the clock is configured as output, the default output frequency is set to 3.072 MHz. For details, see the *IA61x API Guide* for flexibility on using PDM clock as an output.

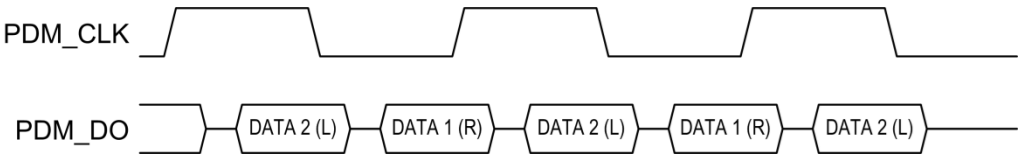


Figure 5 PDM Two-Channel Output Timing

Table 2 Supported PDM Clock Rates

PDM Clock (kHz)	Recommended Max Bandwidth of Audio Signal (kHz)
512	8
768	8
1024	10.66
1536	16
2048	21.33
2400	25
3072	32
4608	48
4800	50

3.2.5.2 *I²S/TDM Digital Audio Port*

When in I²S+ I²C or I²S+UART mode, the IA610 can transfer audio data using the I²S or TDM protocol with an external host or codec device. (Table 18, on page 31, lists the pin configuration in these modes.) Using API commands, the IA610 can be configured to operate either in slave or master mode.

I²S transfers have the following features.

- Bit clock (I2S_CLK) up to 24.576 MHz.
- Sampling clock (I2S_WS) up to 192 kHz.
- There must be exactly two slots, Left (I2S_WS low) and Right (I2S_WS high).
- There must be an equal number of I2S_CLK periods in each half I2S_WS period.
- Support for 8 to 32 audio data bits per slot (channel).

Figure 6 shows an example of I²S mode.

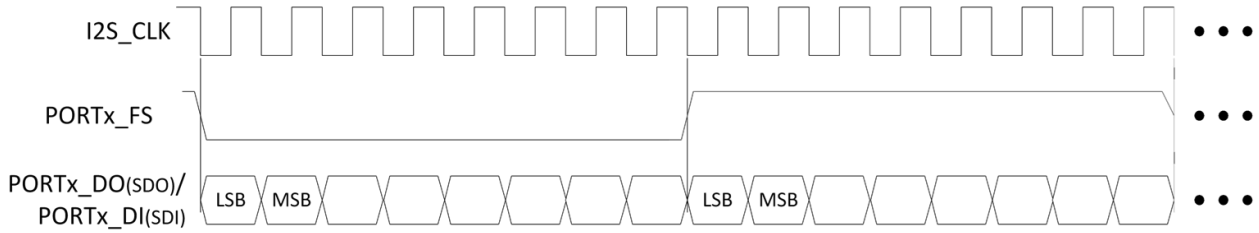


Figure 6 I²S Mode

TDM transfers have the following features.

- Bit clock (I2S_CLK) up to 24.576 MHz.
- Sampling rates of up to 192 kHz.
- Frame Sync pulse (I2S_WS) must be at least one bit-clock wide.
- Support for up to four active slots (channels) out of 32. Slots do not need to be contiguous. In master mode, the master clock generator supports up to 256 clocks per frame, but slave TDM operation is not limited by clocks per frame, and supports up to 32 slots with 32 data bits per slot.
- Support for 8 to 32 audio data bits per slot (channel).
- Support for output transmission on either rising or falling bit clock edge.
- Support for input sampling on either rising or falling bit clock edge.
- Transmitting and sampling edges must be of opposite polarity.
- Support for both MSb-first and LSb-first transmission modes.

Figure 7 shows an example of TDM mode.

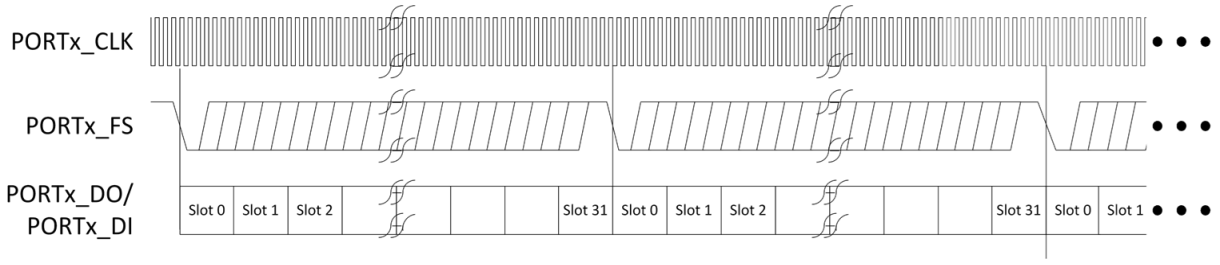


Figure 7 TDM Mode

3.2.6 Host Interfaces

3.2.6.1 *Firmware Download, Command and Control*

The IA610 audio processor supports command and control over the following interfaces.

- SPI up to 13 Mbps.
- UART up to 2.048 MBaud.
- I²C up to 1 MHz.

3.2.6.2 *SPI*

The IA610 supports a four-wire Serial Peripheral Interface (SPI) protocol up to 13 Mbps. The SPI slave port can be used to download a firmware image onto the IA610 and to send API control and data to the IA610.

3.2.6.3 *UART*

The IA610 supports a two-wire UART (UART_TX, UART_RX). The UART can be used to download a firmware image onto the IA610, and a UART connection to the host is required for streaming as alternative to ID tapping. The interface can detect the baud rate automatically up to 115 kHz; it also supports baud rates of 0.4608, 0.9216, 1.000, 1.024, 1.152, 2.000, and 2.048 MHz, as configured by the host using the Bootloader UART baud rate change API command, or by the firmware after the binary file has been downloaded.

3.2.6.4 *I²C*

The IA610 supports a Slave I²C bus as the host interface with a seven-bit address range. The I²C address can be set through the data output Latch On Reset (LOR) configuration pin, as described in Section 5.1.3.3, Latch On Reset Configuration Pins. The I²C interface can be used to download a firmware image onto the IA610.

3.2.6.5 *Debug*

The collection of diagnostic data streams is supported on the SPI, UART, I²C interfaces. This requires the ability to collect synchronized input/output streams using any of the interfaces.

Debug is supported either by a virtual connection over ADB to an Android Proxy running on the host processor, or by a direct physical connection to test-points on the system PCB, with no-load resistors connected to the SPI, UART, or I²C I/O pins.

3.3 **System Control Unit**

3.3.1 Boot Control

Upon the supply of power to VDD pin, the IA610 goes through a power-up initialization process. During this, the IA610 does not respond to host requests. The IA610 then enters an auto-detect mode for control interfaces to determine which pin configuration to use for operation. See Section 4.7.1 for more information on the start-up sequence; see the *IA61x API Guide* for more information on the auto-detect sequence.

3.3.2 Reset Control

The IA610 has no external reset pin; it generates an internal reset signal on initial power-up, after receipt of a reset command from the host, or on detection of any communication issues through the use of an on-board watchdog timer. The IA610 has a variety of low-power modes it can enter and exit without requiring a reboot and re-download of system firmware (see Section Chapter 4:). Thus, it is recommended that the IA610 supply voltage be left on all of the time. Power Management

3.3.3 Power Management

The block diagram in Figure 3 color codes the different power domains of the IA610. There are three primary power domains: one to supply the bias of the MEMS element, one to supply the core analog signal path circuitry, and one to supply the core DSP subsystem. The DSP core subsystem has three subordinate power domains that can be independently controlled to optimize power in various use cases. This section provides further details around the primary ASIC power domains.

Table 3 Power Supply Pins

Name	Voltage	Max Current	Power Direction	Comment
GND	0 V	25 mA	—	
VDD	1.8 V	25 mA	Input	Main microphone IO supply.
LDO	0.6 V – 1.2 V	23 mA	Output	Primary supply for DSP functions of the microphone.

where:

GND is the common ground pin for all IA610.
VDD provides power to all I/Os, as well as the power management blocks (LDOs) in the Smartmic.
LDOD provides the power output for the DSP subsystem, including the processor, memory, Audio Fabric, and core logic. The output can range from 0.6 V to 1.2 V.

3.4 Clock Control

3.4.1 PLL

The IA610 has an integrated, high-performance Phase Lock Loop (PLL) that provides clocks for the processors, memory, and core logic circuits; it also provides oversampling clocks that drive the serial control communications interfaces. See Table 9 for performance details of the PLL.

3.4.2 Internal Oscillators

The IA610 has two integrated silicon oscillators: one optimized for low-power, the other optimized for accuracy and system flexibility.

3.4.2.1 Low-Power Oscillator

The low-power oscillator is calibrated at the factory, and the output frequency is always set to 768 kHz. This oscillator is specifically designed for low-power voice-wake modes.

3.4.2.2 *High-Performance Oscillator*

The high-performance oscillator is also calibrated at the factory, and the output frequency is set to 43.008 MHz. This output frequency can be divided down by counters within the IA610 for use by various internal modules, or for use as a master output clock. See Table 10, on page 23, for performance details of this oscillator.

3.5 Interrupts

The IA610 provides an interrupt request to the host for a keyword detection event through the HOST_IRQ function, as well as a wakeup event from the host through the WAKE function.

The HOST_IRQ and WAKE function maps to a particular pin based on the configuration; see Table 18 on page 31, as well as the *IA61x API Guide* for more information.

Chapter 4: Operating Modes

The IA610 can be in one of the following operating modes.

- Bootloader Auto-Detect Mode — After power up, the IA610 detects the host control interface and waits for firmware download.
- Voice Wake Mode — The IA610 is in low-power mode and can detect spoken keywords.
- Software Pass-Through Mode — The IA610 acts as a left- or right-channel PDM or I^2S mic to the host.
- Hardware Pass-Through Mode — The IA610 acts as a PDM mic with duplicated PDM signals on the left and right channels.
- Retention-Sleep Mode — The IA610 is in a very low-power state where memory is retained.
- Deep-Sleep Mode — The IA160 is in its lowest power state (with power enabled). Memory is not retained.

4.1 Bootloader Mode (SBL)

Upon system power-up, or after deep-sleep mode, the IA610 is in Bootloader Mode and waits for either an API command to determine the host control interface, or a PDM clock to enter HW Bypass Mode. Once the control interface is determined, firmware can be downloaded by the host and configured to put the IA610 into one of the other listed modes. See the *IA61x API Guide* for details on auto-detecting the control interface, firmware download, and mode switching.

4.2 Voice Wake Mode

The Voice Wake feature on the IA610 processor provides low-power voice wake-up based on detection of either a pre-defined keyword (OEM keyword), or a user-trained OEM keyword (Voice ID). The host can go into a very-low-power mode and wait for the IA610 to sense activity and wake it up.

In Voice Wake mode, the IA610 monitors the microphone stream for acoustic activity in an ultra-low-power mode. When acoustic activity is detected, the IA610 automatically enters into a slightly higher power mode to analyze the speech utterance for the presence of the wake-up keyword. When a valid keyword is detected, the IA610 asserts an interrupt to the host processor to trigger complete system wake-up. If a keyword is not detected, the device returns to the ultra-low power mode until acoustic activity is detected again. The timeline for this is shown in Figure 8.

Due to its ultra-low-power, Voice Wake enables an always-on touchless user interface for mobile device or IoT wake-up.

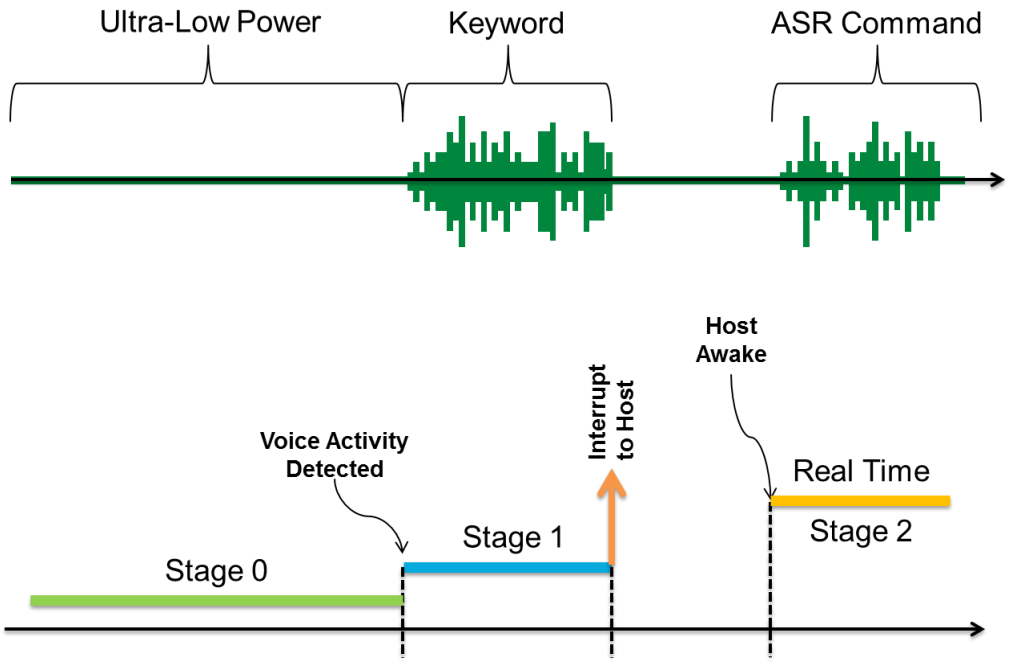


Figure 8 Timeline in Voice Wake Mode

4.2.1 Wake-Up Trigger Types

Voice Wake keeps the mobile device in a low-power, always-on listening mode, in which the device is listening for the wake-up trigger. Once the trigger is detected, the device wakes up and performs the desired action. Voice Wake offers the choice of OEM-selectable, user-selectable, or user-dependent OEM wake-up triggers.

4.2.1.1 *OEM Selectable Wake-Up Triggers*

With this option, OEMs can select a keyword to wake the device. This wake-up trigger wakes up the mobile device whenever a user says this word. This OEM-selectable trigger is speaker-independent and does not require user training.

4.2.1.2 *User Dependent OEM Wake-Up Triggers (VoiceID)*

With this option, users can train their device to only wake up to their voice when speaking the OEM keyword. In this mode, the user trains the system by speaking the OEM key phrase several times in a relatively quiet environment. The OEM-selectable trigger then is speaker-dependent, which means that once a user has trained the system to his or her voice, the system recognizes and responds only to that voice.

4.3 **Continuous Voice Wake**

The Continuous Voice Wake feature starts where the Voice Wake feature leaves off, and buffers up to two seconds[1] of audio on the IA610 device after receiving the wake-up trigger. It then passes this speech (and optionally also the keyword) to the automated speech recognition (ASR) engine running on the host processor. This allows the host processor time to properly perform its own wakeup and startup sequence to ultimately receive audio data for the remainder of the command. Continuous Voice Wake allows devices to continuously listen to their surroundings, wake up upon a simple, configurable voice keyphrase, and act on

[1] Buffer size varies based on use-case and algorithm used.

the instructions that follow without any significant delay between keyword and subsequent command phrase.

For example: Hello Voice Q, what is the weather like today?

The IA610 is part of a larger system that includes the Codec, Host Application Processor, and Baseband processor, along with peripheral control busses, such as UART and SPI, which connect them. Continuous Voice Wake is performed by the system as a whole in the following stages.

Stage 0 (AAD Mode): The IA610 is in ultra-low power Acoustic Activity Detection mode. SmartMic listens for acoustic input and only wakes up the main processor when the acoustic level is above the threshold.

Stage 1 (Keyword Detect Mode): The IA610 is in low-power mode and processing inbound microphone samples for the presence of one of the pre-loaded keywords. When a keyword is detected, the IA610 generates an interrupt to the Host, then saves some relevant state information. The IA610 then transitions to stage 2.

Stage 2 (Burst Mode): While the host is waking up, the IA610 continues buffering mic data in a circular audio buffer. Once the host is running, it can start bursting the audio buffer over SPI/UART/I²S/ I²C. Once the host stops the capture, it can put the IA610 back into stage 0 (Voice Wake Mode) or Pass-Through Mode. Figure 9 shows this timeline.

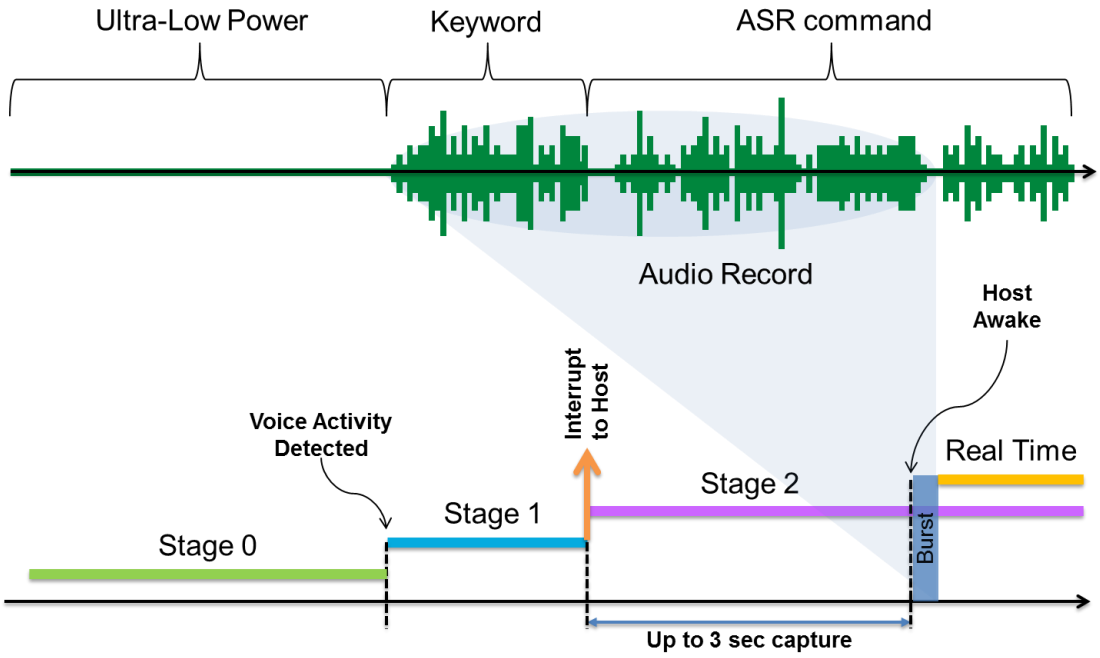


Figure 9 Continuous Voice Wake System Timeline

4.3.1 Keyword Preservation

Continuous Voice Wake can be configured to maintain the 16 kHz keyword and pass it to the host with the buffer. This allows for secondary host-based inspection of the keyword, as well as ASR channel estimation. Due to the memory needed to keep the keyword, enabling this feature limits the number of available keywords.

4.4 Software Pass-Through

The IA610 can be in software pass-through mode, in which case it acts as a left- or right-channel PDM or I²S mic to the host. Software Pass-Through mode is supported only after firmware download.

4.5 Hardware Pass-Through

Hardware Pass-Through allows the host to put the IA610 in a low-power digital audio pass-through mode to bypass processing. In this mode, the IA610 acts as a PDM mic with duplicated PDM signals on the left and right channels.

4.6 Low-Power Modes

Retention and deep sleep modes are used when audio data from IA610 is not required. They are the lowest power modes of the IA610. The difference between them is: retention mode maintains firmware code on the device (at the expense of additional power consumption); deep sleep mode requires firmware re-download during a transition to an active mode.

4.6.1 Deep Sleep Mode

Deep Sleep mode can be entered after the firmware has been downloaded. When the chip enters into sleep mode, the memory content is not retained. A wakeup signal from deep sleep is required to bring the chip into boot loader (SBL) mode. A firmware download is needed after the wakeup from deep sleep mode. Exiting deep sleep requires all internal hardware blocks to restart. This is the lowest power mode of the IA610.

4.6.2 Retention Sleep Mode

Retention Sleep mode can be entered after the firmware has been downloaded. The chip enters into normal sleep mode, and the memory content is retained. A wakeup signal from retention sleep mode is required to bring the chip into firmware mode. A firmware download is not needed after the wakeup from retention sleep mode. Exiting retention sleep restarts all internal hardware blocks that were powered off due to the sleep command.

4.7 Operating Sequences

4.7.1 Start-Up Sequencing

Figure 10 shows a complete start-up sequence, including system power and the host bus.

After Latch On Reset, the IA610 wakes up in the Auto-detect state, determines the control interface, and waits for command communication or firmware download from the host.

Note that the host interface pins MUST be driven to ground during VDD power-up so that they are never at a higher voltage than VDD+0.3 V.

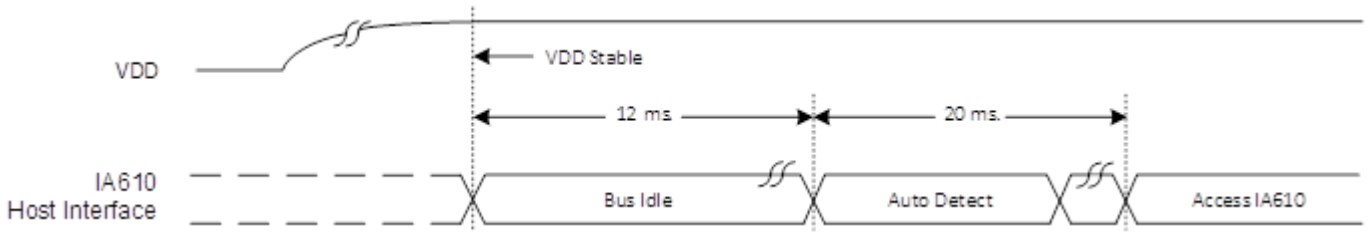


Figure 10 Start-Up Sequence

The host MUST follow a defined sequence to download program code into the IA610. The *IA61x API Guide* provides a detailed description of program code download sequences over the various interfaces.

4.7.2 Sleep and Wake-up Sequence

The IA610 can be placed into an ultra-low-power sleep state to minimize power consumption. During sleep, the host can continue to access other devices connected to the host interface buses.

Figure 11, Figure 12, and Table 4 provide a general overview of the sleep and wake-up process and their timings. The *IA61x API Guide* provides a detailed description of the sleep and wake-up sequences.

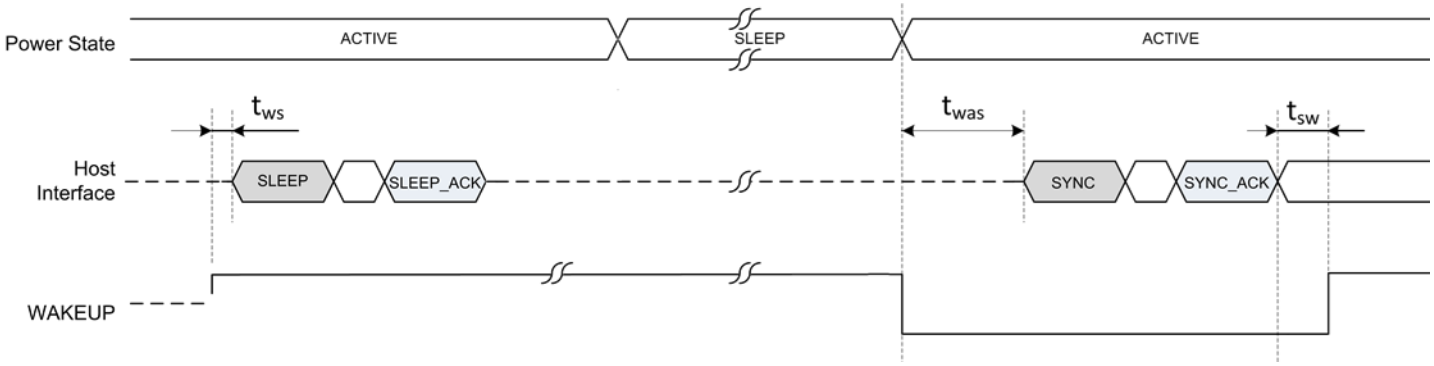


Figure 11 Sleep and Wake-Up Sequence for Waking Up the IA610 Using the WAKEUP Input

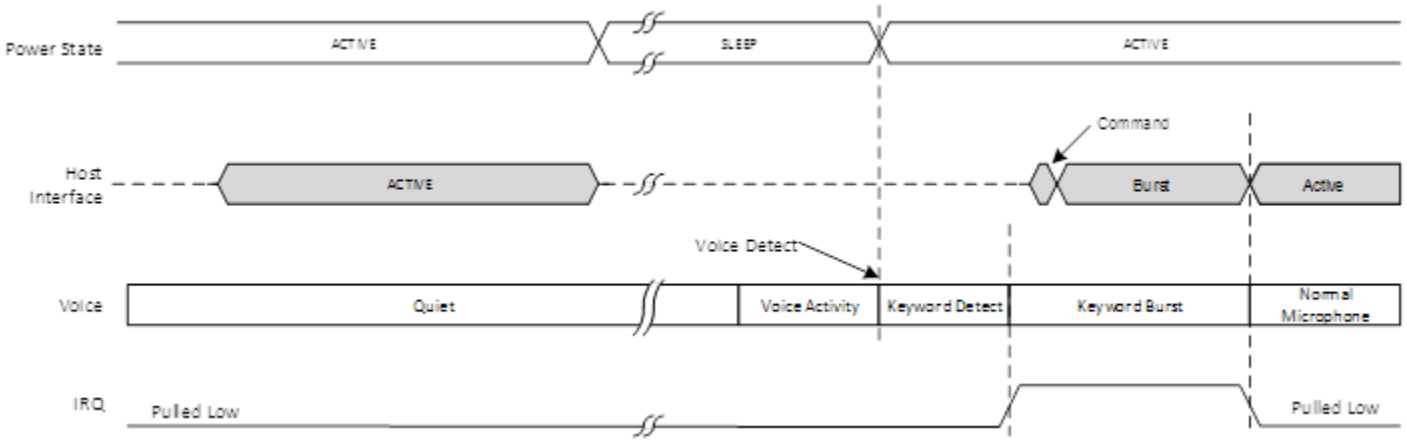


Figure 12 Sleep and Wake-up Sequence for Voice Wake Mode

Table 4 Sleep and Wake-up Sequence Timings

Parameter	Symbol	Min	Typ	Max	Units
Time from WAKEUP deasserted to SLEEP command write	tws	30	-	-	ms
Time from WAKEUP asserted to SYNC command write	twas	30	-	-	ms
Time from SYNC _ACK read to WAKEUP deasserted	tsw	0	-	-	ms

4.7.3 State Diagram

The IA610 state diagram is shown in Figure 13.

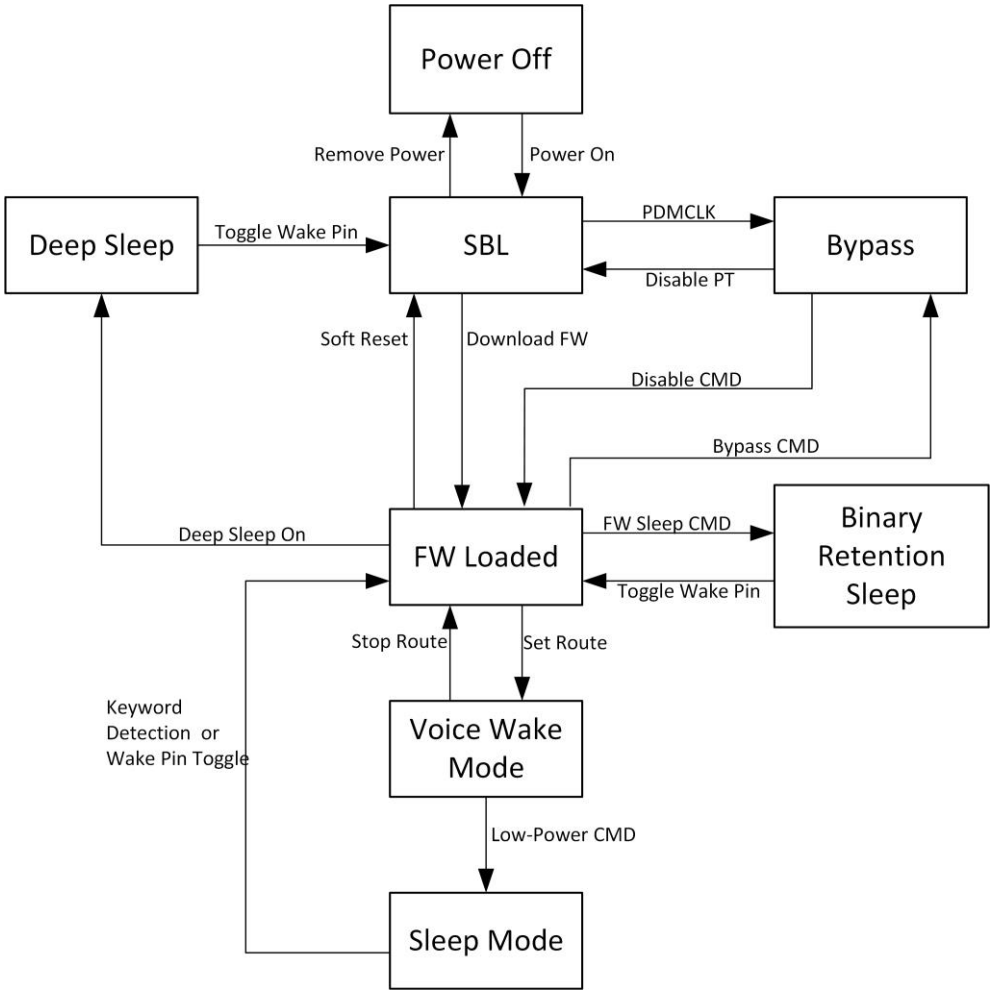


Figure 13 IA610 State Diagram

Chapter 5: Acoustic and Electrical Specifications

Table 5 General Specifications

Test Conditions: Vdd=1.8 V, No Load, T_A = 25° C, 55±20% R.H., PDM+SPI mode, 3.072 MHz clock, unless otherwise indicated.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	VDD		1.71	1.8	1.89	V
Low-Frequency Roll-Off	LFRO	-3 dB relative to 1 kHz	-	41	-	Hz
		-3 dB relative to 1 kHz (768 kHz PDM clock)	-	95	-	
High Frequency Flatness		+3dB relative to 1kHz	-	14	-	kHz
Resonant Frequency Peak	Fres	Free Field response	-	28	-	kHz
DC Offset		Fullscale= +-100	-	0	-	%FS
Directivity			Omnidirectional			
Polarity		Increasing sound pressure	Increasing density of 1's			
Sensitivity Drop		Vdd(min) <=Vdd <=Vdd(max)	-	-	+-0.25	dB
DC Output		Fullscale = ±100	-	0	-	% FS
Bandwidth	BW	-3 dB relative to 1 kHz	-	50	-	kHz
Functional Operating Temperature	T_A		-40	25	85	ºC

Table 6 Normal Mode

Test Conditions: Vdd=1.8 V, No Load, T_A = 25° C, 55±20% R.H., PDM+SPI mode, 3.072 MHz clock, unless otherwise indicated.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Current	IDD	Voice Wake Burst Mode (stage 2)	-	7.5	-	mA
		Hardware Pass-Through Mode		1.74		
Sensitivity[1]	S	94 dB SPL @ 1 kHz	-38	-37	-36	dBFS
Signal to Noise Ratio	SNR	94 dB SPL @ 1 kHz, A-weighted	-	65.5	-	dB(A)
Total Harmonic Distortion	THD	94 dB SPL @ 1 kHz, S = Typ	-	0.15	0.5	%
Acoustic Overload Point	AOP	1% THD @ 1 kHz, S = Typ	-	114.5	-	dB SPL
		10% THD @ 1 kHz, S = Typ		132.5		
Power Supply Rejection Ratio	PSRR	200 mVpp sinewave @1 kHz	-	87	-	dBV/FS
Power Supply Rejection	PSR+N	200 mVpp 7/8 duty cycle rectangular waveform @ 217 Hz, A-weighted	-	-96	-	dBFS(A)

[1] 100% tested.

Table 7 Low-Power Mode

Test Conditions: Vdd=1.8 V, No Load, T_A = 25° C, 55±20% R.H., PDM+SPI mode, 768 kHz clock, unless otherwise indicated.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Current[1]	IDD	Deep Sleep Mode	-	0.32	-	mA
		Voice Wake AAD Mode (stage 0)	-	0.40	-	
		Voice Wake Keyword Detect Mode (stage 1)		1.12		
		Hardware Pass-Through Mode		0.74		
Sensitivity[1]	S	94 dB SPL @ 1 kHz	-22	-21	-20	dBFS
Signal to Noise Ratio	SNR	94 dB SPL @ 1 kHz, A-weighted	-	64.5	-	dB(A)
Total Harmonic Distortion	THD	94 dB SPL @ 1 kHz, S = Typ	-	0.15	0.5	%
Acoustic Overload Point	AOP	1% THD @ 1 kHz, S = Typ	-	113	-	dB SPL
		10% THD @ 1 kHz, S = Typ	-	116.5	-	
Power Supply Rejection Ratio	PSRR	200 mVpp sinewave @1 kHz	-	71	-	dBV/FS
Power Supply Rejection	PSR+N	200 mVpp 7/8 duty cycle rectangular waveform @ 217 Hz, A-weighted	-	-80	-	dBFS(A)

[1] 100% tested.

Table 8 Electrical Characteristics

Test Conditions: Vdd=1.8 V, T_A = 25° C, unless otherwise indicated

Parameter	Symbol	Min	Typ	Max	Units
Digital Input High-Level Voltage	V_{IH}	0.65*VDD			V
Digital Input Low-Level Voltage	V_{IL}	-0.2		0.35*VDD	V
Digital Output High-Level Voltage	V_{OH}	0.65*VDD			V
Digital Output Low-Level Voltage	V_{OL}			0.35*VDD	V
Programmable Digital Input Internal Pull-Down Resistor		35	61	114	kΩ
Programmable Digital Input Internal Pull-Up Resistor		39	71	138	kΩ
I/O drive strength (default)		7	12	17.5	mA
Capacitance To Ground of I/O Pins	C	9		18	pF

Note: Maximum output current source or sink drive by any I/O pin is programmable in four steps. The default is 4 mA nominal. See the *IA61x API Guide* for details and settings.

Note: External I/O loading and drive strength have a direct effect on voltage V_{IH} and V_{IL} transition times. For timing critical signals, the values of any external R and C components connected to the I/O pins must be adjusted based on the application.

The PLL has two frequency ranges of operation, set through the software API. PFD refers to the Phase-Frequency Detector on the PLL, which receives a divided-down version of the reference clock.

Table 9 PLL Characteristics

Test Conditions: Vdd=1.8 V, at TA = 25° C, unless otherwise indicated

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Reference Frequency	f_{PLL_IN}		0.768		200	MHz
PFD Frequency	f_{PLL_PFD}	Low Range	0.768		$f_{PLL\_VCO} \div 4$	MHz
		High Range	0.768		$f_{PLL\_VCO} \div 8$	MHz
VCO Frequency	f_{PLL_VCO}	Low Range	28		140	MHz
		High Range	120		600	MHz
Output Frequency	f_{PLL_OUT}		0.11		600	MHz
Lock Time	t_{PLL_LOCK}		500		1000	PFD cycles
Feedback Divider	n_{PLL_FBDIV}		4		781	Integer
Loop Bandwidth	f_{PLL_BW}			$f_{PLL\_PFD}/25$		MHz
Period Jitter (random)	$t_{PLL\_JIT\_RND}$	f_{PLL_VCO} = 50 MHz		$0.7\ pS \times \sqrt{\frac{600\ MHz}{f_{PLL\_VCO}}} \times \sqrt{\frac{600\ MHz}{f_{PLL\_OUT}}}$	8.4	pS (RMS)
Period Jitter Power Supply Noise Sensitivity	$t_{PLL\_JIT\_PS}$			1.5		pS/mV
Period Jitter from Reference Spur	$t_{PLL\_JIT\_REF}$			1%		Output clock cycle

The on-chip silicon oscillator, which is calibrated in the factory, has two ranges of operation, set by internal register through the software API.

Table 10 Oscillator Characteristics

Test Conditions: Vdd=1.8 V, at TA = 25° C, unless otherwise indicated.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Frequency	f_{OSC_OUT}	Low Range		43.008		MHz
		High Range		172.032		
Output Frequency Temperature Dependence	Δ_{OSC_T}	0 to 80°C		340	535	ppm/°C
Period Jitter (random)	$t_{OSC\_JIT\_RND}$	Low Range			44	pS (RMS)
		High Range			22	
Period Jitter Power Supply Noise Sensitivity	$t_{OSC\_JIT\_PS}$	Low Range		0.9	2.2	pS/mV

5.1 Digital Interfaces

5.1.1 Audio Port Interface Characteristics

5.1.1.1 *I²S/TDM Interface Slave Timing*

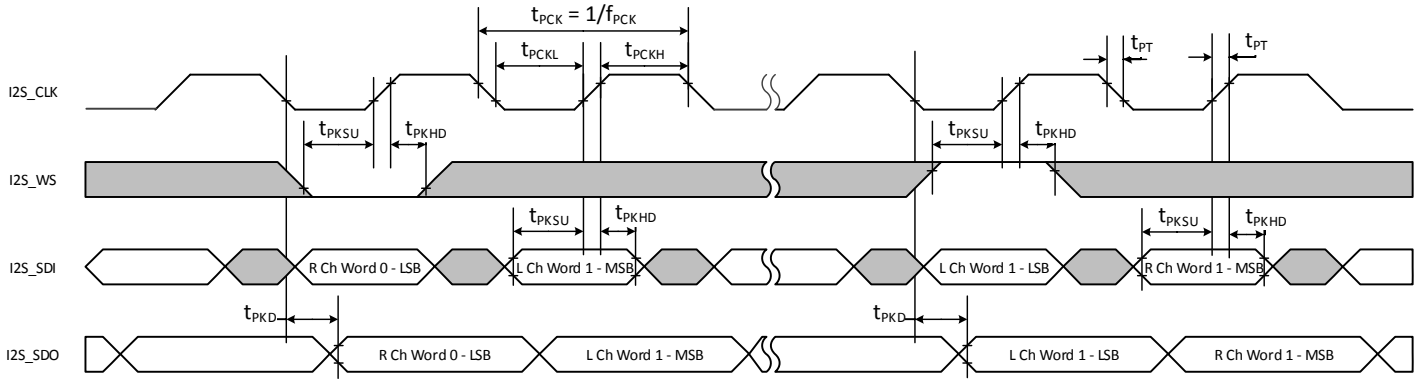


Figure 14 I2S/TDM Interface Slave Timing

In Slave Mode, I2S_CLK and I2S_WS are inputs.

Table 11 I²S/TDM Slave Timing

Test Conditions: VDD = 1.8V, 10pF Load, at T_A =25° C, unless otherwise specified. Measurement levels on waveforms are Vih and Vil. Note 1

Parameter	Symbol	Min	Typ	Max	Units
I2S_CLK Clock Frequency	f_{PCK}			24.576	MHz
I2S_CLK Clock Cycle Time	t_{PCK}		$1/f_{PCK}$		s
I2S_CLK Clock High Pulse Width	t_{PCKH}	35			% t_{PCK}
I2S_CLK Clock Low Pulse Width	t_{PCKL}	35			% t_{PCK}
I2S input transition time	t_{PT}		10		ns
I2S_SDI and I2S_WS Input Setup Time to CLK ↑ Note 2	t_{PKSU}	25			ns
I2S_SDI and I2S_WS Input Hold Time from CLK ↑ Note 2	t_{PKHD}	5.1			ns
I2S_SDO Data Output Delay from CLK ↓ Note 3	t_{PKD}	0		15	ns

Note 1: Timing parameters are guaranteed by design; they are not tested in the final test.
Note 2: The I2S_WS and I2S_SDI inputs are set to be sampled at the rising edge of the I2S_CLK.
Note 3: The I2S_SDO outputs are set to drive at the falling edge of the I2S_CLK.

5.1.1.2 *I²S/TDM Interface Master Timing*

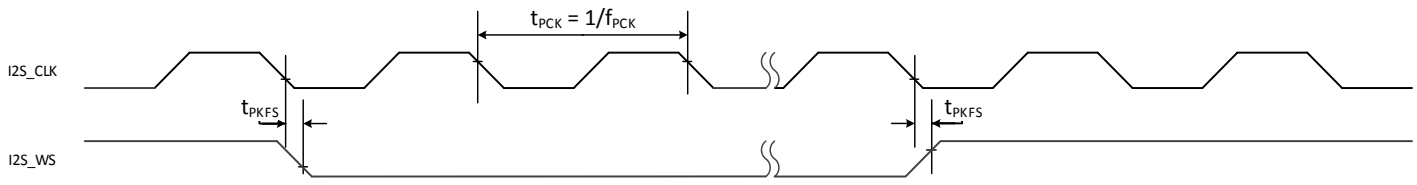


Figure 15 I²S/TDM Interface Master Timing

In Master mode, I2S_CLK and I2S_WS are outputs, but I2S_SDI and I2S_SDO timing with respect to I2S_CLK is identical to that for Slave mode.

Table 12 I²S/TDM Master Timing

Test Conditions: VDD = 1.8 V, 10 pF Load, at T_A =25° C, unless otherwise specified. Measurement levels on waveforms are Vih and Vil. Note 1

Parameter	Symbol	Min	Typ	Max	Units
I2S_WS Output Delay from CLK ↓ *Note 2*	t_{PKFS}	0		25%	t_{PCK}

Note 1: Timing parameters are guaranteed by design; they are not tested in the final test.
Note 2: The I2S_WS outputs are set to drive at the falling edge of the I2S_CLK. Delay from CLK ↓ to I2S_CLK is determined by an integer number of periods of an internal oversampling clock used to generate both I2S_CLK and I2S_WS.

5.1.2 Audio Port PDM Interface Characteristics

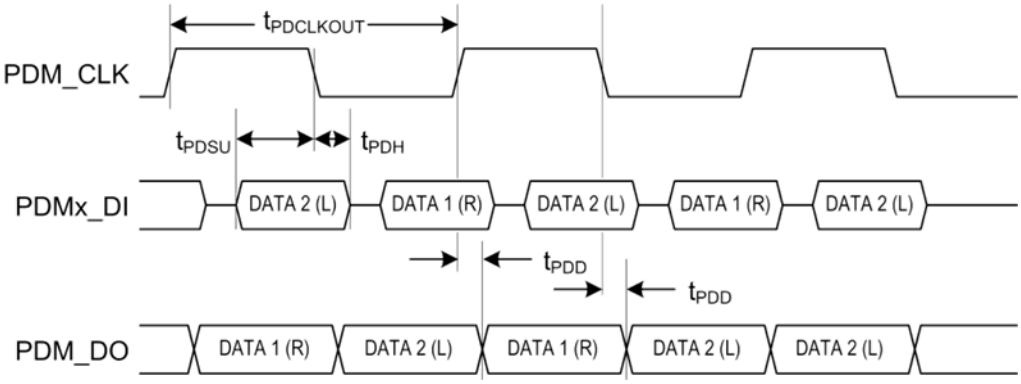


Figure 16 PDM Interface Timing

Table 13 PDM Timing

Test Conditions: VDD = 1.8 V, 10 pF Load, at T_A =25° C, unless otherwise specified

Parameter	Symbol	Min	Typ	Max	Units
PDM_CLK Output Frequency, Operating	$f_{PDCLKOUT}$	0.512	3.072	4.800	MHz
PDM_CLK Output Frequency, Low-power Voice Wake Mode		0.512	0.768 Nominal		MHz
PDM Data Input Setup Time to Clock Edge	t_{PDSU}	25			ns
PDM Data Input Hold Time after Clock Edge	t_{PDH}	3			ns
PDM Data Delay from PDM_CLK Edge [2]	t_{PDD}	6			ns

Note 1: Timing parameters are guaranteed by design; they are not tested in the final test.
Note 2: The edge of the clock on which data is output is programmable.

5.1.3 Control Interfaces

5.1.3.1 *UART*

The IA610 supports a two-wire UART (UART_SIN, UART_SOUT). The UART can be used to download a firmware image onto the IA610, and a UART connection to the host is required for streaming as alternative to ID tapping. The interface can detect the baud rate automatically up to 115 kHz; it also supports baud rates of 0.4608, 0.9216, 1.000, 1.024, 1.152, 2.000, and 2.048 MHz as configured by the host using the Bootloader UART baud rate change API command, or by the firmware after the binary file has been downloaded.

5.1.3.2 *I²C Interfafce*

The IA610 supports a Slave I²C bus as the host interface with a seven-bit address range. The I²C address can be set through the data output Latch On Reset (LOR) configuration pin, as described in Section 5.1.3.3. The I²C interface can be used to download a firmware image onto the IA610.

5.1.3.3 *Latch On Reset Configuration Pins*

The IA610 contains two Latch On Reset (LOR) address pins that set the I²C slave address when in I²C mode. The state of the address pins is latched when power is on and stable. An internal pull-down resistor pulls the address pins low (0) when unconnected. To set the address pin to a logical value of 1, connect the LOR pin to the same power supply that powers the IA610 with an external 10 kΩ pull-up resistor.

Table 14 shows the configuration of the address pins and the resulting I²C address.

Table 14 Latch On Reset Configuration for I²C Address

ADDR1	ADDR2	Description
0	0	7 bit, address 0x3E (default)
0	1	7 bit, address 0x38
1	0	7 bit, address 0x3F
1	1	7 bit, address 0x39

5.1.4 I²C Slave Timing

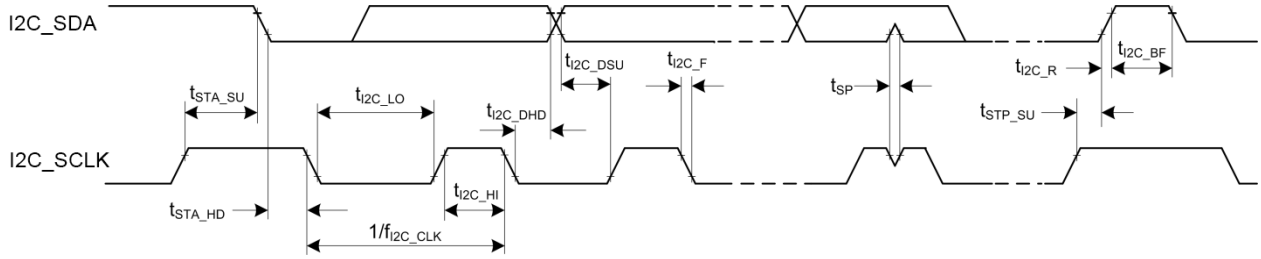


Figure 17 I²C Slave Interface Timing

Table 15 I²C Slave Timing

Test Conditions: VDD = 1.8 V, 10 pF Load, at T_A =25° C, unless otherwise specified.

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode+		Units
		Min	Max	Min	Max	Min	Max	
I²C Clock Frequency	f_{I2C_CLK}	0	100	0	400	0	1000	kHz
I²C Clock High Period	t_{I2C_HI}	4.0		0.6		0.26		µs
I²C Clock Low Period	t_{I2C_LO}	4.7		1.3		0.5		µs
Start Condition Setup Time	t_{STA_SU}	4.7		0.6		0.26		µs
Start Condition Hold Time	t_{STA_HD}	4.0		0.6		0.26		µs
Stop Condition Setup Time	t_{STP_SU}	4.0		0.6		0.26		µs
Bus Free Time between Stop and Start Conditions	t_{I2C_BF}	4.7		1.3		0.5		µs
I²C Clock and Data Rise Time	t_{I2C_R}	-	1000	20	300	-	120	ns
I²C Clock and Data Fall Time	t_{I2C_F}		300		300		120	ns
I²C Data Setup Time	t_{I2C_DSU}	250		100		50		ns
I²C Data Hold Time	t_{I2C_DHD}	0	202	0	202	0	-	ns
Spike Suppression Period	t_{SP}	0	0	0	50	0	50	ns

5.1.5 SPI Interface Characteristics

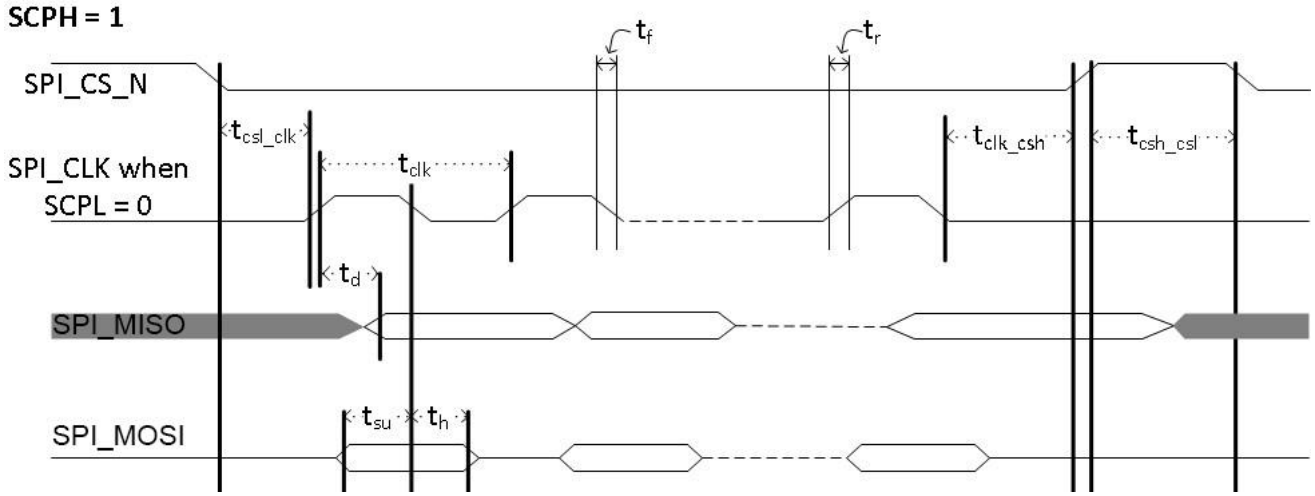


Figure 18 SPI Interface Timing

On reset, the SPI clock phase is set to SCPH=1, and the clock polarity is set to SCPL=0 in bootloader auto-detect mode. The SPI interface is 32-bit. See the IA61x API Guide for enabling the SPI interface in bootloader mode.

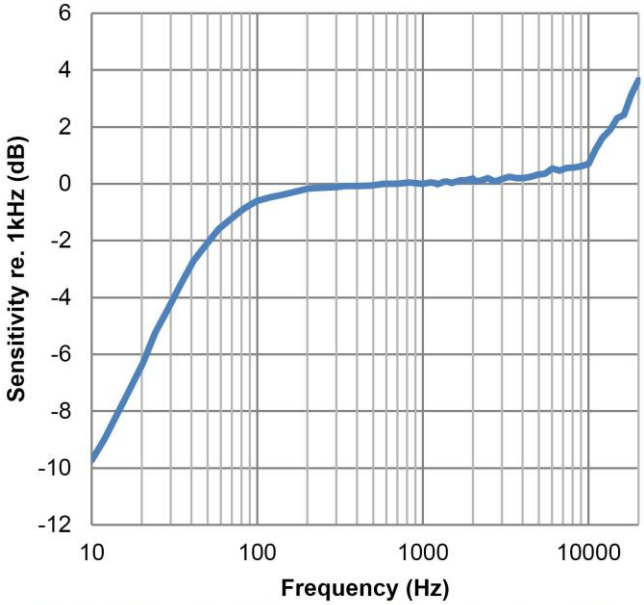
Table 16 SPI Timing SCPH = 1

Test Conditions: VDD = 1.8V, >=6x oversampling, 10pF Load, at T_A = 25° C, unless otherwise specified.

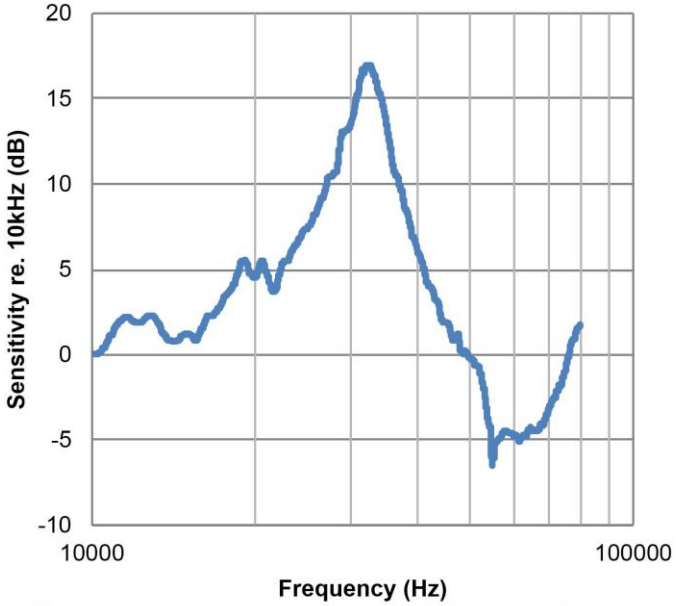
Parameter	Symbol	Min	Typ	Max	Units
SPI sample clock frequency	f_{samp}	-		43	MHz
SPI sample clock period	T_{samp}	23.25		-	ns
SPI clock frequency	f_{clk}	-		13	MHz
SPI clock period	t_{clk}	76.92		-	ns
Chip select assert to clock edge	t_{csl_clk}	1		-	t_{clk}
Clock edge to chip select de-assert	t_{clk_csh}	1		-	t_{clk}
Chip select de-assert to chip select assert	t_{csh_csl}	1		-	t_{clk}
Tx data valid from clock edge	t_d	-		64.125	ns
Rx data setup time	t_{su}	0.5		-	t_{samp}
Rx data hold time	t_h	1.5		-	t_{samp}
SPI clock rise time	t_r	-		10%	t_{clk}
SPI clock fall time	t_f	-		10%	t_{clk}

Chapter 6: PERFORMANCE CURVES

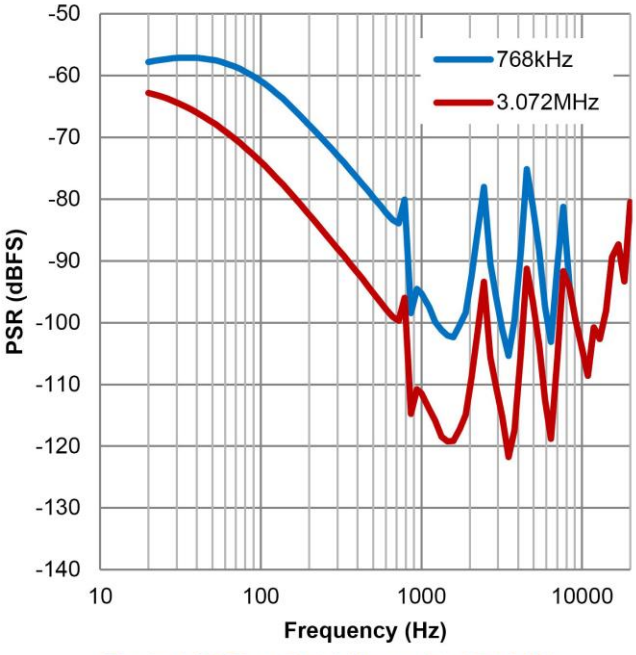
Test Conditions: VDD = 1.8 V; No Load; at T_A =25° C; 55±20% R.H.; Hardware Pass-Through Mode, unless otherwise specified.



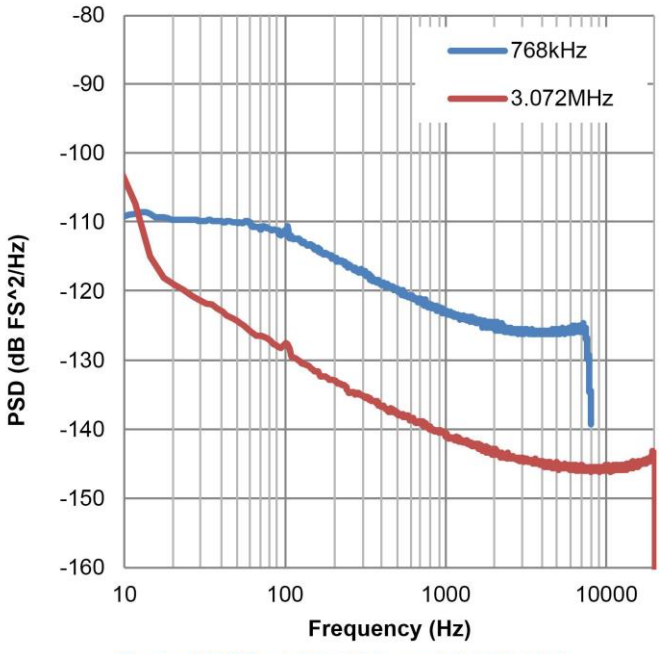
Typical Free Field Response Normalized to 1 kHz



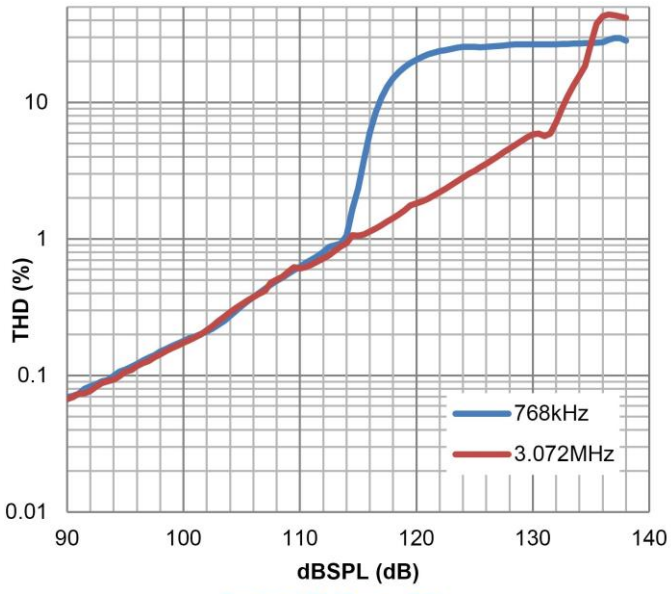
Typical Free Field Response Normalized to 10 kHz



Typical PSR at 768 kHz and 3.072 MHz



Typical PSD at 768 kHz and 3.072 MHz



Typical THD vs. SPL

Chapter 7: Pin Descriptions

7.1 Pinout Diagram

Figure 19 shows the pinouts for the IA610 (bottom view).

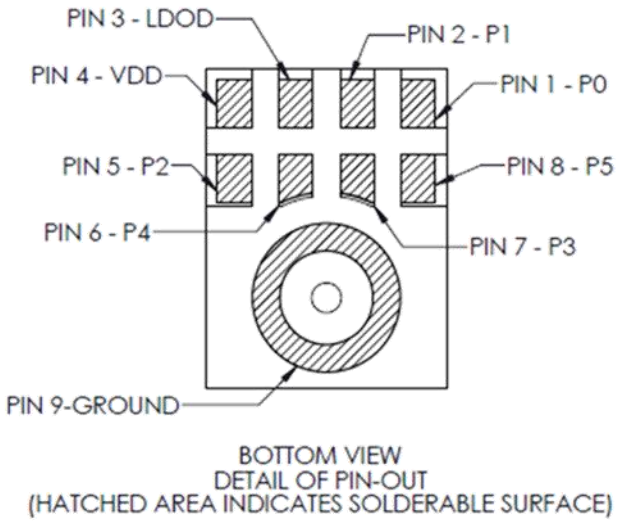


Figure 19 Pin Assignments (Bottom View)

7.2 Pinout Table

Table 17 shows a list of the IA610 pins and the signals associated with them. In active mode, the pin state is set by firmware and differs from mode to mode. Firmware can configure a pin as an input or an output; it also can enable internal pull-ups or pull-downs, if available.

Table 17 Pin Descriptions

Pin#	Name	Type	Description
1	P0	Digital I/O	P0 I/O
2	P1	Digital I/O	P1 I/O
3	LDOD	Power	Connect to Bypass Capacitor
4	VDD	Power	Power Supply
5	P2	Digital I/O	P2 I/O
6	P4	Digital I/O	P4 I/O
7	P3	Digital I/O	P3 I/O
8	P5	Digital I/O	P5 I/O
9	GND	Power	Ground

Table 18 Pin Configuration Per Boot Mode

Mode	P0	P1	P2	P3	P4	P5	IRQ	WAKE
PDM + I2C	PDM_CLK	PDM_SDO	I2C_ADDR1 WAKE	I2C_ADDR2 IRQ	I2C_SCLK	I2C_SDA	P3	P2
PDM + UART	PDM_CLK	PDM_SDO	NA	IRQ	UART_RX WAKE	UART_TX	P3	P4
PDM + SPI	PDM_CLK	PDM_SDO IRQ	SPI_SCLK	SPI_MISO	SPI_SS WAKE	SPI_MOSI	P1	P4
I2S + I2C	I2S_WS	I2S_CLK	I2S_SDI I2C_ADDR1 WAKE	I2S_SDO I2C_ADDR2 IRQ	I2C_SCLK	I2C_SDA	P3	P2
I2S + UART	I2S_WS	I2S_CLK	I2S_SDI	I2S_SDO IRQ*	UART_RX WAKE	UART_TX IRQ*	P3	P4

* IRQ can be configured to be on either I2S_SDO or UART_TX, depending on the configuration settings.

Chapter 8: Mechanical Specifications

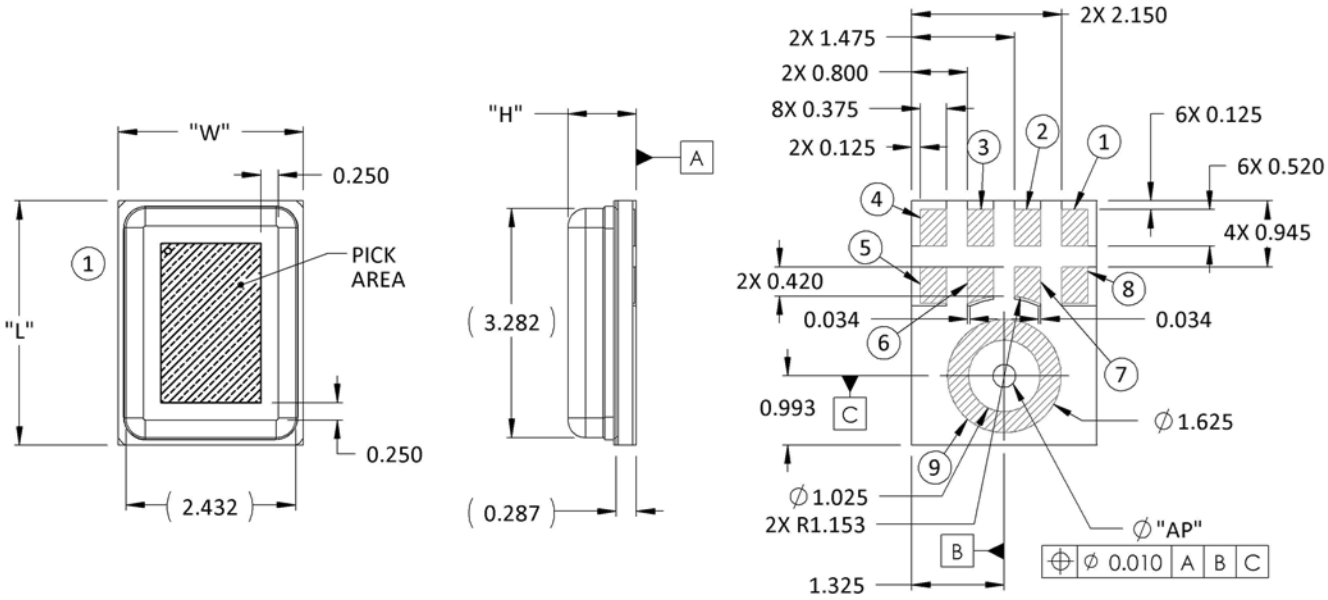


Table 19 Mechanical Specifications

Item	Dimension	Tolerance	Units
Length (L)	3.50	±0.10	mm
Width (W)	2.65	±0.10	mm
Height (H)	0.98	±0.10	mm
Acoustic Port (AP)	0.325	±0.05	mm

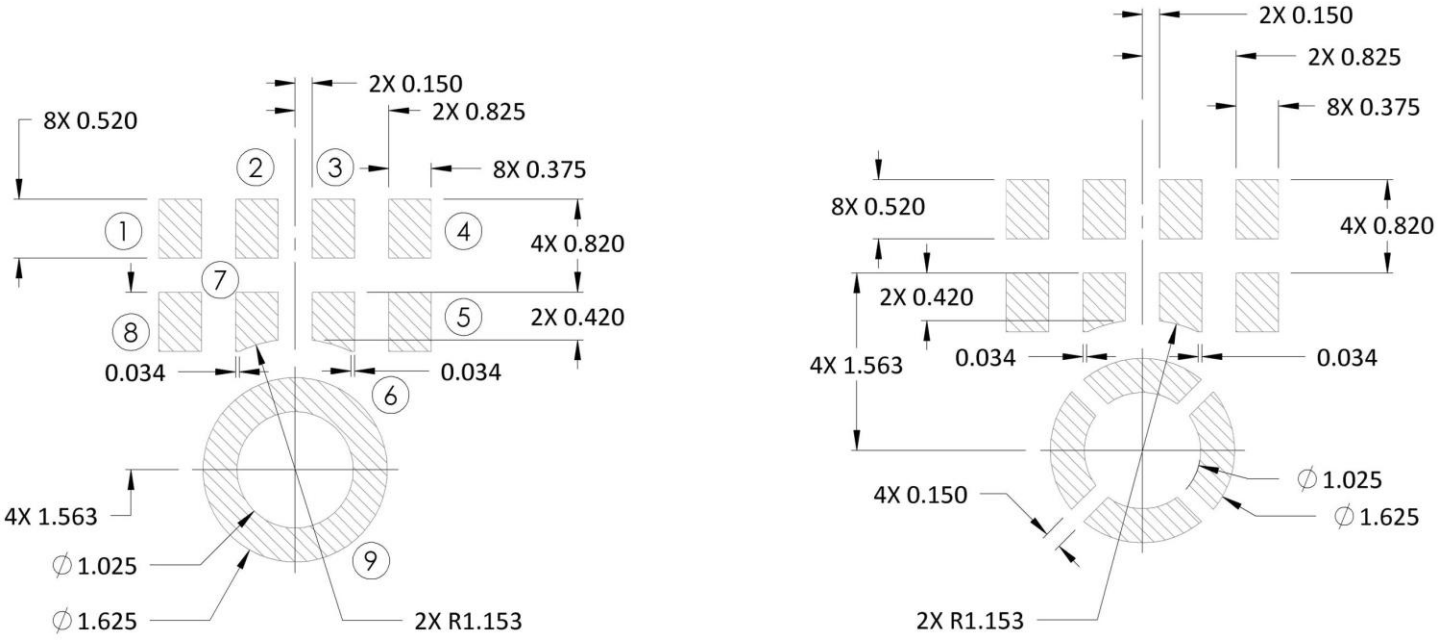


Figure 20 Example of Land Pattern (left) and Stencil Pattern (right)

Chapter 9: Packaging and Marking Details

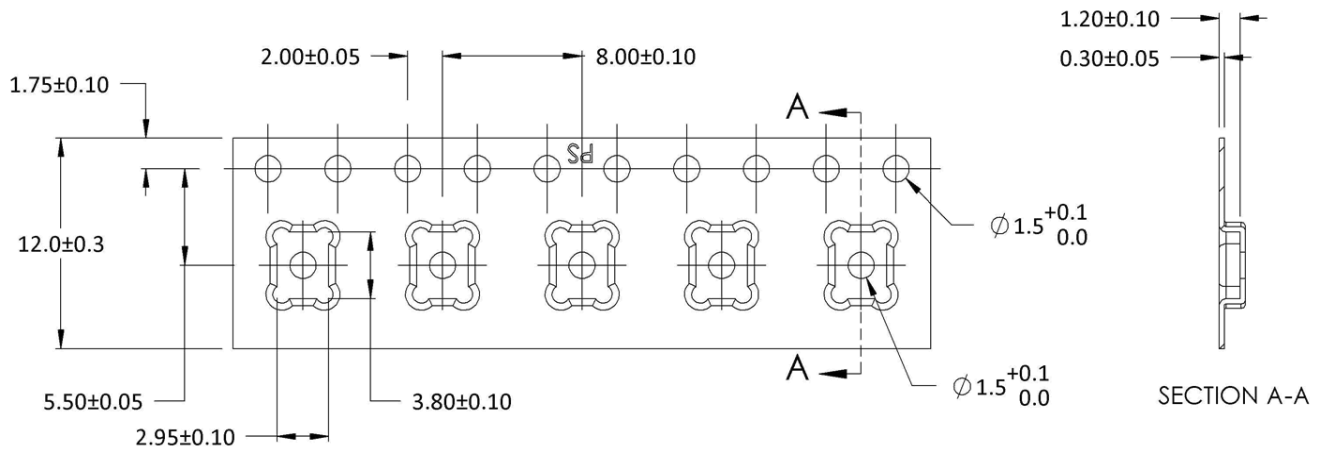
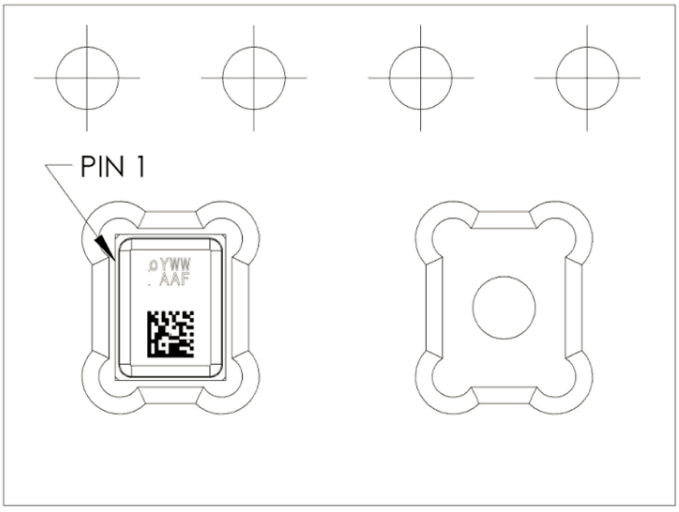


Table 20 Model and Part Numbers

Model Number	Part Number	Quantity Per Reel
IA610	SPH0671LM7H	5,900



Date Code YWW:
Y: Last digit of year
WW: Work week

AA = Project Name Designator:
AD: Shapiro
AE: Shapiro Soundwire

F = Factory Location:
M: Knowles Factory KEM3
C: Knowles Factory KES2
P: Knowles KEI

2D barcode serial number: PPPYWWDMSSSSAARD
PPP = Vendor/Facility code
KEM = FF9
KES = FMV
KEI = FF8
Y = Last digit of current year
WW = Work week
D = Day, Sunday is 1 and Saturday is 7
MSSSS = 5 digit serial code
M = Machine ID for laser
SSSS = Base 34 serial number
(Do not use letter I or O)
AA = Project name designator
AD: Shapiro
AE: Shapiro Soundwire
R = Revision number
D = Development Stage
E = Engineering Sample
P = Prototype Sample
M = Mass production

Notes: Dimensions are in millimeters unless, otherwise specified.
Vacuum pickup only in the pick area indicated in Mechanical Specifications.
Tape and reel per EIA-481.
Labels are applied directly to reel and external package.
Shelf life: Twelve (12) months when devices are to be stored in factory supplied, unopened ESD moisture-sensitive bag under maximum environmental conditions of 30°C, 70% R.H.

Chapter 10: Recommended Reflow Profile

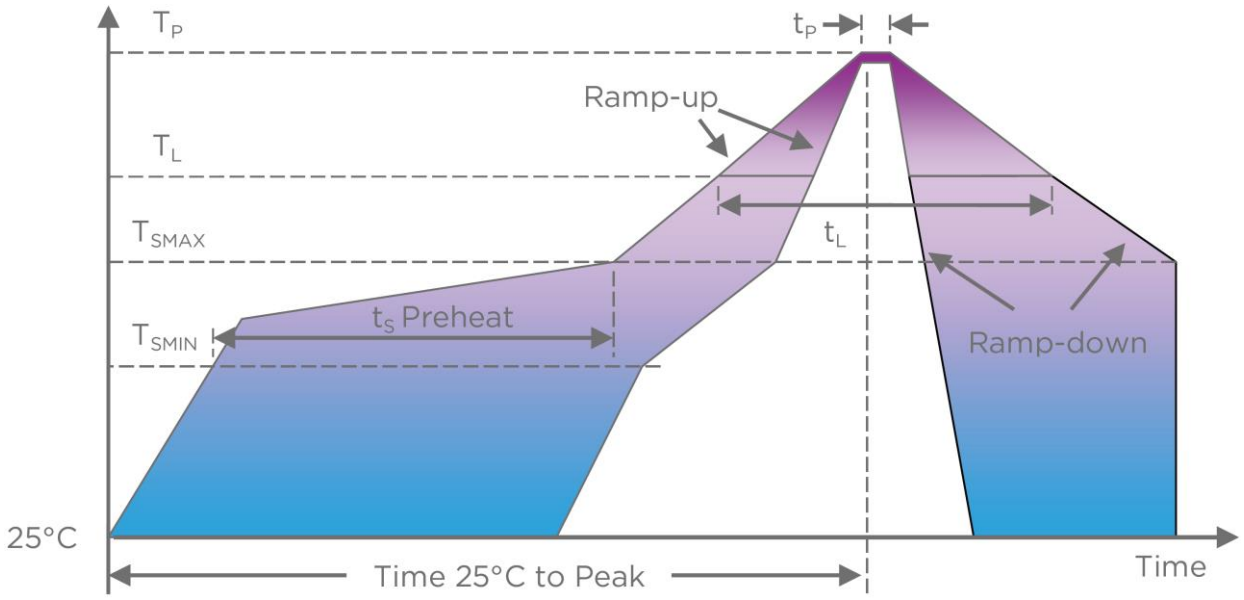


Figure 21 Recommended Reflow Profile

Table 21 Profile Specifications

Profile Feature	Pb-Free
Average Ramp-up rate (T_{SMAX} to T_P)	3°C/second max.
Preheat Temperature Min (T_{SMIN}) Temperature Max (T_{SMAX}) Time (T_{SMIN} to T_{SMAX}) (t_S)	 150°C 200°C 60-180 seconds
Time maintained above: Temperature (T_L) Time (t_L)	 217°C 60-150 seconds
Peak Temperature (T_P)	260°C
Time within 5°C of actual Peak Temperature (t_P)	20-40 seconds
Ramp-down rate (T_P to T_{SMAX})	6°C/second max
Time 25°C to Peak Temperature	8 minutes max

Notes: Based on IPC/JDEC J-STD-020 Revision C.
All temperatures refer to topside of the package, measured on the package body surface.
(A) MSL (moisture sensitivity level) Class 1.
(B) Maximum of 3 reflow cycles is recommended.
(C) In order to minimize device damage:

- Do not board wash or clean after the reflow process.
- Do not brush board with or without solvents after the reflow process.
- Do not directly expose to ultrasonic processing, welding, or cleaning.
- Do not insert any object in port hole of device at any time.
- Do not apply over 30 psi of air pressure into the port hole.
- Do not pull a vacuum over port hole of the microphone.
- Do not apply a vacuum when repacking into sealed bags at a rate faster than 0.5 atm/sec.

Chapter 11: PCB Design and Layout Guidelines

11.1 Power Planes

Power supply noise can have a significant impact on the performance of analog circuitry in the system. Use low impedance power planes with decoupling capacitors for the system power supply design.

Place ceramic SMT bypass capacitors (1 µF) next to the IA610 VDD power input pin, as well as the LDOD pin (see Figure 22). Additional decoupling capacitors (0.1 µF) may be necessary to reduce the noise on the power pin. Keep routing traces for the decoupling capacitors as short as possible. A long trace has an antenna effect that can introduce additional noise into the power supply, which requires additional filtering.

11.2 Digital Signal Routing

Follow good design practices in the PCB layout by keeping the digital signal traces as short as possible and away from analog and RF signals.

11.3 Typical Application

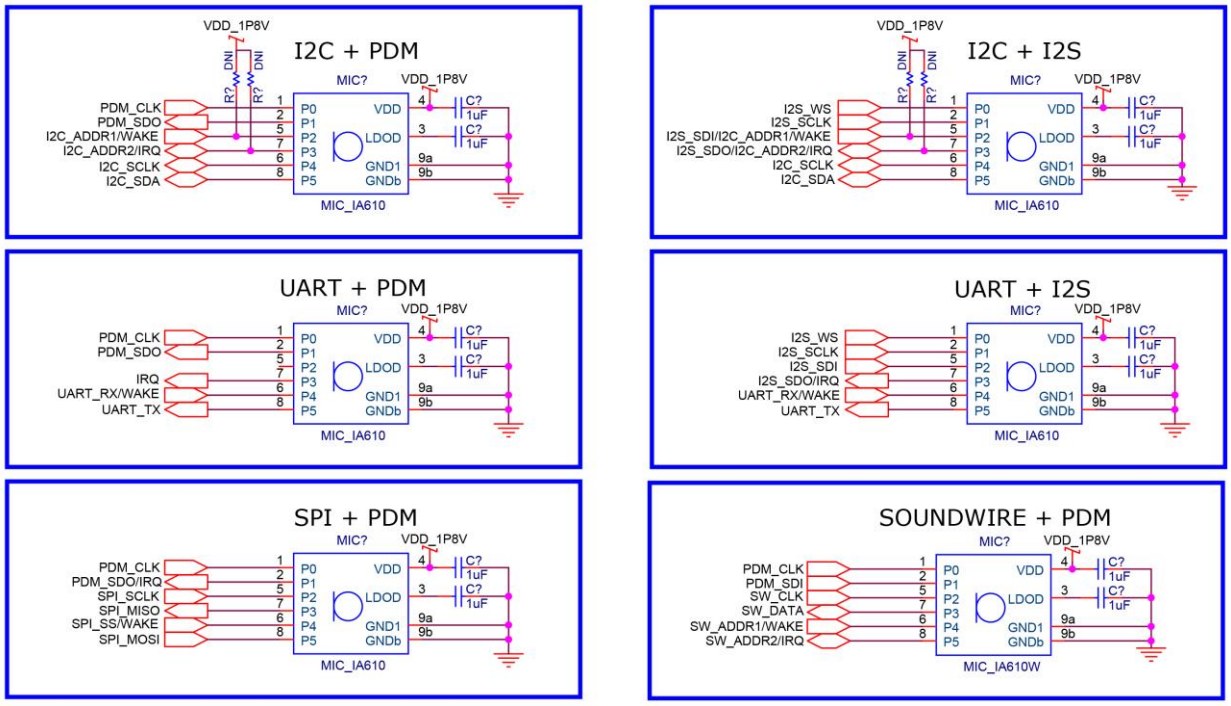


Figure 22 Schematics Showing Connection for Each of the Various Interface Configurations

Chapter 12: Materials Statement

Meets the requirements of the European RoHS directive 2011/65/EC as amended.

Meets the requirements of the industry standard IEC 61249-2-21:2003 for halogenated substances and Knowles Green Materials Standards Policy section on Halogen-Free.

Product is Beryllium Free according to limits specified on the Knowles Hazardous Material List (HSL for Products).

Ozone depleting substances are not used in the product or the processes used to make the product, including compounds listed in Annex A, B, and C of the "Montreal Protocol on Substances That Deplete the Ozone Layer.

Chapter 13: Reliability Specifications

Table 22 Reliability Test Specifications

Test	Description
Thermal Shock	100 cycles of air-air thermal shock from -40°C to +125°C with 15 minute soaks (IEC 68-2-4)
High Temperature Storage	+105°C environment for 1,000 hours (IEC 68-2-2 Test Ba)
Low Temperature Storage	-40°C environment for 1,000 hours (IEC 68-2-1 Test Aa)
High Temperature Bias	+105°C environment while under bias for 1,000 hours (IEC 68-2-2 Test Ba)
Low Temperature Bias	-40°C environment while under bias for 1,000 hours (IEC 68-2-1 Test Aa)
Temperature/Humidity Bias	+85°C/85% R.H. environment while under bias for 1,000 hours (JESD22-A101A-B)
Vibration	16 minutes in each X, Y, Z axis from 20 to 2,000 Hz with peak acceleration of 20 G (MIL 883E, Method 2007.2,A)
ESD-HBM	3 discharges of ±2kV direct contact to I/O pins (MIL 883E, Method 3015.7)
ESD-LID/GND	3 discharges of ±8kV direct contact to lid while unit is grounded (IEC 61000-4-2)
ESD-MM	3 discharges of ±200V direct contact to IO pins (ESD STM5.2)
Reflow	5 reflow cycles with peak temperature of +260°C
Tumble Test	300 Random Drops of Test Box on to Steel Base from 1.0m, 10 Tumbles/Minute
Mechanical Shock	3 pulses of 10,000 G in each of the X, Y, and Z directions (IEC 68-2-27 Test Ea)

Notes:
Microphones meet all acoustic and electrical specifications before and after reliability testing, except sensitivity, which can deviate up to 3 dB.
After three reflow cycles, the sensitivity of the microphones shall not deviate more than 1 dB from its initial value.

Revision History

Revision	Description	Date
1.0	Initial release.	21-Mar-2019

Knowles Corporation
1151 Maplewood Drive
Itasca, Illinois 60143

Phone: (630) 250-5100
Fax: (630) 250-0575
info@knowles.com

Model/Reference Number:
AUD-ESP-00458, Rev 1.0